Sigma Delta ADCs
Specifications

- Programmable Sigma-Delta ADC
  - Input sample rate: 48KHz
  - 16bit resolution
    - Switchable to 96KHz@15bits, 192KHz@14bits
- 45nm technology: 1V
- Input current range: ±5μA
Current vs. Voltage Mode

- Input current allows use of capacitor as integrator, rather than op-amp integrator
- Savings in area and complexity
- Requires use of voltage to current converter
Dealing With Overflow

- $2^n$ cycles per sampling period, but counter limited to $2^{n-1}$ levels

- Three proposed solutions:
  - Make sure not to overload input
  - Sample before last cycle so overflow never appears at the output
  - Add an overflow bit (requires either an extra bit or one bit less resolution)
Mixed Signal Synthesis

- Create custom analog cell(s) with standard cell height
- Generate abstract view from layout
- Generate LEF file, append to standard cell LEF file
- Synthesize digital section normally (behavioral Verilog), place and route using timing optimization
- Combine analog and digital circuits using structural Verilog
- Re-run place and route without timing optimization
Modulator Output
Decimator Simulation
Placed Cells
Placed and Routed
Cell Count and Area

Analog circuit area of ~15μm² versus ~500μm² for full circuit (3%)
Netlist Extraction and Simulation

- OpenAccess for easy management
- Procedure:
  - Extract netlist with Calibre
  - Attach netlist to symbol
  - Simulate with ADE
Programmability

- Oversampling ratio = $\frac{\text{bitstream\_clock}}{\text{sample\_rate}}$
- With fixed bitstream clock, can trade between sample rate and resolution (through oversampling ratio)
Verilog Code

Decimator Behavioral Verilog

```verilog
module decimator16bit (CLK, VMOD, MODE, Q);
  input CLK, VMOD, MODE;
  output [15:0] Q;
  reg [15:0] count, timer, Q;
  
  always @(posedge CLK)
  begin
    timer = timer + 1'b1;
    if(timer == 16'hffff && MODE == 1'b0)
      Q <= count;
    if(timer == 16'h8000 && MODE == 1'b1)
      Q <= count;
  end

  always @(negedge CLK)
  begin
    if (timer == 16'hffff && MODE == 1'b0)
      count = 16'h0000;
    else if(timer == 16'h8000 && MODE == 1'b1)
      count = 16'h0000;
    else if(VMOD)
      count = count + 1'b1;
  end

  endmodule
```

ADC Structural Verilog

```verilog
module adc16bit(IN, CLK, MODE, OUT);
  input IN, CLK, MODE;
  output [15:0] OUT;
  wire IN, CLK, VMOD, MODE;
  wire [15:0] OUT;
  decimator16bit decimator1
    (.CLK (CLK), .VMOD (VMOD), .MODE (MODE), .Q (OUT));
  modulatorL mod1(.IN (IN), .CLK (CLK), .OUT (VMOD));
  endmodule
```
Deliverables

- Current mode Sigma Delta modulator schematics
- Programmable decimator verilog code
- Placed and routed ADC layout
- Simulation results and design metrics