Power Management in Ultra-Low Power Systems

PhD Proposal

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Abhishek Roy
Motivation

GROWTH IN THE INTERNET OF THINGS
THE NUMBER OF CONNECTED DEVICES WILL EXCEED 50 BILLION BY 2020

Source: Cisco
Motivation for Ultra-low Power (ULP) systems

- System integration
- Small form-factors
- Longer operational lifetime for ubiquitous deployment

=> Need for Energy Harvesting and Power Management System

Source: http://inertia.ece.virginia.edu/engineering-research/body-area-sensor-networks
Block Diagram of a BSN SoC

- Supported Applications:
  - Activity detection and logging
  - Energy expenditure
  - Fall detection
  - Temperature tracking
  - Heart rate monitoring and fibrillation detection
  - Long-term data monitoring and statistics
  - Posture
  - Motion-artifact removal

Source: Klinefelter et al. ISSCC 2015
Proposed Contributions

Source: Klinefelter et al. ISSCC 2015
Thesis Statement(s)

By employing the following features in the power management infrastructure of an IoT SoC:

- Fully integrated energy harvesting from multiple energy sources
- Fully integrated power-efficient supply voltage regulation
- Controlling power supply variation
- ULP digital/mixed-signal circuit components

Significant advantages at the system-level such as:

- Energy-autonomy and near-perpetual system operation
- A longer operational lifetime
- Smaller overall form-factor
- System flexibility and use in a wide range of applications
Outline

- Energy Harvesting
- Supply voltage regulation
- Monitoring Power supply variation
- Ultra-low-power analog/digital circuit components
- Timeline and Publications
Outline

- Energy Harvesting
  - Supply voltage regulation
  - Monitoring Power supply variation
  - Ultra-low-power analog/digital circuit components
- Timeline and Publications
Energy Harvesting: Background

- Circuits which:
  - Extracts energy from ambient sources such as:
    - Thermal energy
    - Photovoltaic
  - Stores energy on a storage device such as a supercapacitor or
  - Uses the energy to charge a battery
Sources of Ambient Energy

Photovoltaic

- Photoelectric Effect
- $I_L \propto \text{Light Intensity}$

Thermal

- Seebeck Effect
- $V_{TEG} \propto \Delta T$

Source: http://www.esru.strath.ac.uk/Courseware/Class-16110/Images/pv1.jpg
Source: Digi-key
## Sources of Ambient Energy

<table>
<thead>
<tr>
<th>Source</th>
<th>Power Density</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Light</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Indoor</td>
<td>100 µW/cm²</td>
<td>Illumination from artificial light</td>
</tr>
<tr>
<td>Outdoor</td>
<td>10 mW/cm²</td>
<td>Natural sunlight</td>
</tr>
<tr>
<td>Thermal Energy</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human</td>
<td>100 µW/cm²@ 5°C gradient</td>
<td>Thermal gradient between body heat and ambient</td>
</tr>
<tr>
<td>Industrial</td>
<td>3.5 mW/cm²@ 35°C gradient</td>
<td>Thermal gradient between machine heat and ambient</td>
</tr>
</tbody>
</table>

Source: Adapted from Tan and Panda, IEEE Transactions on Industrial Electronics, 2011

=>$\textbf{Extremely low available power}$ for harvesting in case of indoor applications and wearables
Need for Energy Storage


=> **Energy storage** is necessary to meet peak current demands of the system

=> **Battery** provides higher energy density, a **supercapacitor** provides greater charge-discharge cycles

<table>
<thead>
<tr>
<th>Source</th>
<th>Battery</th>
<th>Supercapacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Li-ion</td>
<td>Thin film</td>
</tr>
<tr>
<td>Operating Voltage (V)</td>
<td>3-3.7</td>
<td>3.7</td>
</tr>
<tr>
<td>Energy Density (Wh/l)</td>
<td>435</td>
<td>&lt; 50</td>
</tr>
<tr>
<td>Self-discharge rate (%/month) at 20°C</td>
<td>0.1-1</td>
<td>0.1-1</td>
</tr>
<tr>
<td>Cycle life (cycles)</td>
<td>2000</td>
<td>&gt; 1000</td>
</tr>
<tr>
<td>Temperature range (°C)</td>
<td>-20/50</td>
<td>-20/70</td>
</tr>
</tbody>
</table>
Energy Harvesting: Background

- Types of energy harvesting architectures:
  - Inductor-based
  - Charge pumps or Switched-capacitor based

- Control Scheme consists of:
  - Maximum Power Point Tracking (MPPT)
  - Low-voltage start-up scheme

- Powertrain-specific components such as:
  - ULP comparators for peak-inductor current control and zero crossing detection
  - Non-overlapping clock generators, level shifters
  - Digital Logic
Factors impacting \( \eta \)

- Conduction loss in the inductor (parasitic DCR), \( M_{HS} \) and \( M_{LS} \)
- Switching loss due to turning ON/OFF \( M_{HS} \) and \( M_{LS} \); gate-control circuits
- Leakage in \( M_{HS} \) and \( M_{LS} \); control circuits

\[
\frac{V_{STORE}}{V_{IN}} = 1 + \frac{T_{LS}}{T_{HS}}
\]

\[
\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{STORE} I_{CAP}}{V_{IN} I_{IN}}
\]
Switched-capacitor based Boost Converters

Factors impacting $\eta$

- Topology
- Conduction loss in the switches and transfer capacitors
- Bottom plate parasitic capacitance
- Switching loss due to turning ON/OFF switches; gate control circuits
- Contention currents in switch control, level shifters; leakage in switches

\[
\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}I_{OUT}}{V_{IN}I_{IN}}
\]
Maximum Power Point Tracking (MPPT)

⇒ MPP of solar and TEG are different fractions of open-circuit voltage

⇒ MPP of solar cell changes with light intensity


Source: Kadirvel et al. “Power Management Functions for energy harvesting”, EETimes 2012
Low Voltage Start-up

Low output voltage from TEGs and indoor solar cells due to:

- Smaller size; Constrained form factors
- Limited temperature differential, Light intensity

⇒ Low output voltage from TEG/solar cell

- Self-Powered system ⇒ No secondary power source

⇒ Need a low-voltage startup circuit to begin energy-harvesting.
⇒ Efficiency is not critical at startup
Energy Harvesting: Prior Work

- Supports TEG or PV (Not both together)
- Cold-start oscillator and RF kickstart
- Fractional o.c. MPPT

⇒ External passives
⇒ At a time only TEG or PV.
Configure $V_{\text{MPP}}$ externally

Source: Shrivastava et al. JSSC 2015
Energy Harvesting: Problem Statement and Hypothesis

**Problem Statement:**

Battery-less ULP systems, which harvest from a single source of energy have the following limitations:

- Less flexibility
- Less reliability and high risk from complete loss of harvested energy
- Limited operational lifetime.

**Hypothesis:**

By enabling the system to harvest from multiple energy sources, the system can operate reliably over long intervals of time and with changing environmental scenarios, making the system more flexible and fit into a wide range of self-powered applications.
Energy Harvesting: Research Questions

- What kind of powertrain topology would enable the flexibility to harvest from both TEG and indoor solar

- What approach needs to be taken for MPPT in a multi-modal harvesting environment

- What kind of start-up schemes would work best in a multi-modal Energy Harvesting-Power Management Unit (EH-PMU)
Approach

Prior-Work: Chip Testing

Start-Up circuits

TEG/PV Characterization

MATLAB/Spice Modeling

Control circuits: comparators, oscillators, level shifters

MPPT control

Energy Harvesting
EH-PMU Chip-Testing

- Two inductors; Fractional o.c.
- MPPT=>External passives
- Cold-start at 220mV
- Sensitive to PCB layout; lacks controllability and observability

Source: Klinefelter et al. ISSCC 2015
Source: Roy et al. IEEE TBioCAS 2015

3/2/16
Energy Harvesting: Figures of Merit

- Efficiency
- Minimum input voltage
- Output Voltage
- Area
Energy Harvesting: Contributions

- A first-order model, for design space exploration for powertrain topologies.

- A hybrid MPPT control to achieve peak power efficiency for both solar and thermal energy harvesting.

- A start-up circuit/architecture for enabling low-voltage system startup.

- A fully-integrated energy harvesting platform for thermal and solar energy harvesting with low-voltage startup and MPPT.
Outline

- Energy Harvesting
- Supply voltage regulation
- Monitoring Power supply variation
- Ultra-low-power analog/digital circuit components
- Timeline and Publications
Supply Voltage Regulation: Background

- A class of power delivery circuits which:
  - Provides stable, well regulated supply voltages to different components of an SoC
  - Delivers power to the SoC components across different operating modes with maximum efficiency
  - Can be off-chip (PMIC) or on-chip (Integrated Voltage Regulators or IVRs)

=> IVRs are more suitable for systems with constrained form factors
Supply Voltage Regulation: Background

- Types of Voltage Regulators
  - Linear Regulators such as Low-Drop-Out (LDO)
  - Switching Regulators:
    - Inductor-based Buck converter
    - Switched-Capacitor-based Buck converters
Supply Voltage Regulation: LDOs

\[
\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}I_{LOAD}}{V_{STORE}(I_{LOAD} + I_{CONTROL})}
\]

- Can be completely integrated. -> **No off-chip passives**
- No switching noise => good **filter**
- Can **step-down** but **not step-up**. Hence \( V_{OUT} < V_{STORE} \)
- **Low Power-efficiency** for high conversion ratios \( V_{OUT}/V_{STORE} \)
Supply Voltage Regulation: Switching Regulators

Inductor-based Buck Converter

- External passives (Inductor) required
- Performance depends on PCB layout, package parasitics.
- Supports wide-range of conversion ratios

2:1 Switched-Cap based converter

- Completely integrated-> No passives
- Switch-dominated or cap-dominated
- Conversion ratios depend on topology
Voltage References

- Provides stable reference voltage ideally independent of supply voltage and temperature

- Used in analog/mixed signal circuits such as voltage regulators, ADC’s etc.

- Options:
  - Bandgap Reference: ~\( \mu \)W Power, ~1V operation
  - \( \Delta V_T \)–based voltage reference: Low power, sensitive to PVT variations

=> Need Low Voltage, Low Power voltage reference for high power-efficiency power converters and ULP systems
Supply Regulation: Problem Statement and Hypothesis

Challenges:
- Different supply voltages, electrical specs of various circuit components.
- Achieve high efficiency
- Need for off-chip passives and components: ↑cost ↑form-factor
- Reliability and limited operational lifetime.

Hypothesis:
A fully-integrated and a hybrid topology (such as switched-cap + LDO) along with an adaptive supply regulation scheme can provide improvements in
- Overall power-efficiency
- Smaller form-factor and reduced design complexity
Supply Regulation: Research Questions

- Single-stage or cascaded topology?
- How much ripple or power supply variation can be tolerated?
- Trade-offs between strong line regulation vs. power-efficiency?
- Sensitivity of a voltage reference circuit? How much tolerance to power supply variation and temperature?
Approach

Prior-Work: Chip Testing

ULP Voltage Reference

Load Profile characterization

MATLAB/Spice Modeling

Control circuits: comparators, oscillators, level shifters

Powertrain architecture

Supply Regulation
Supply Regulation: Figures of Merit

- Efficiency
- Ripple
- Minimum Input Voltage
- Maximum load current
- Response time
- Area
Supply Regulation: Contributions

- An architecture for supply-regulation targeted at achieving high power efficiency at 1-10µW load comparable or better than the state-of-the-art

- A ULP voltage reference circuit operating at low supply voltage and suitable for light-load regulation.

- A framework or model for evaluating ripple and supply voltage variation vs. efficiency
Outline

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Power Supply Variation: Background

- High Frequency: \( L \frac{di}{dt} \), package resonance
- Low Frequency: Voltage Regulator, IR drop

Adapted from: Muhtaroglu, A.; et al. "On-die droop detector for analog sensing of power supply noise," JSSC 2004
Power Supply Droop Monitors: Prior Work

- On-Die Analog Droop detectors ➔ Higher Quiescent currents
- Adaptive clock distribution and in-situ timing error detection and correction ➔ Area
- Decoupling capacitors ➔ Gate leakage

=> Need low cost, compact, ULP supply voltage droop monitors in high-efficiency voltage regulators for ULP systems
Power Supply Variation: Research Questions

- What architectural methods/circuit techniques/design methodologies provide better power supply noise immunity?

- What bandwidth should an on-die power supply noise detector support?

- How much resolution is acceptable?

- What will be the calibration scheme for measuring power supply noise?
Approach

- Latch vs. Register-based implementation
- ULP droop measurement circuit
- Vector-based Decap insertion
- Supply Variation
- Alternate Decap topologies
All-Digital Power Supply Droop Measurement Unit

- Current-controlled ring oscillator operating at noisy supply
- A counter running at noise-free supply counts RO clock cycles

Source: Roy A. et al. ISCAS 2016
Power Supply Variation: Figures of Merit

- Power Consumption
- Resolution for droop measurement
- Area
Supply Voltage Variation: Contributions

- Evaluating latch-based design implementation flow for better power supply noise immunity

- Low power droop measurement scheme using digital circuits

- Design flow for vector-based dynamic IR analysis and alternate decoupling capacitor (such as active decoupling capacitors) topologies
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Ultra-low-power circuit components

- ULP wakeup-radio system
  - Low-power, low input-referred offset comparators
  - Low-power digital correlators

- ULP Digital circuits in novel process technologies
  - MSP430 processor in MITLL 90nm FDSOI
  - A 16-bit, 32-tap FIR filter in 55nm Deeply Depleted Channel (DDC)
Ultra-low-power wake-up receiver

- 10nW total system power budget ➞ ULP comparator, biasing, digital logic
- 5-10mV rectified output ➞ Need very low input-offset
- ~1V operation
ULP Processing for Wake-up

- 8-bit correlator (n=8)
- 4-bit offset control (M=4)
- Correlator + offset control consumes 3.6nW at 0.5V supply and 10kHz
Approach

Technology: ULP MSP430 in 90nm FDSOI

Technology: FIR filter in 55nm DDC

Alternate logic-styles

ULP ultra-low power Wakeup-receiver

ULP low-offset comparators

ULP circuit components
ULP comparators and digital processing: Figures of Merit

- Power Consumption
- Operating voltage and clock frequency
- Input-referred offset and noise
- Bandwidth
ULP MSP430 Processor in 90nm FDSOI process

- 16-bit MSP430 processor fabricated in 90nm FDSOI

- Process optimized for sub-\(V_T\) operation
  - Reduced \(V_T\) variation
  - Steeper sub-\(V_T\) slope, higher \(I_{ON}/I_{OFF}\)

- Processor consumes 1.3 µW and 5pJ/cycle at 0.4V and 250kHz

Source: Roy A. et al. ISQED 2016
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- Timeline and Publications
# Research Timeline

<table>
<thead>
<tr>
<th>Subject</th>
<th>Task Description</th>
<th>Status</th>
<th>Related Publications</th>
</tr>
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<tbody>
<tr>
<td><strong>Energy harvesting from multiple modalities</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>Architecture exploration and literature review</td>
<td>Completed</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Testing and evaluation of previous baseline architecture</td>
<td>Completed</td>
<td>[AR1][AR2]</td>
</tr>
<tr>
<td>3</td>
<td>Modeling, characterization and design space exploration of harvester topologies, MPPT, start-up</td>
<td>April'16</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Chip tapeout with MPPT and cold-start-Phase I</td>
<td>May'16</td>
<td></td>
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<tr>
<td>5</td>
<td>Chip Testing-Phase I</td>
<td>Oct'16</td>
<td>[AR6]</td>
</tr>
<tr>
<td>6</td>
<td>Chip tapeout with entire multi-modal harvesting system-Phase II</td>
<td>Nov'16</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Chip Testing-Phase II</td>
<td>Mar'17</td>
<td>[AR7][AR10]</td>
</tr>
</tbody>
</table>

| **Voltage Regulation**                 |                                                                                 |              |                      |
| 1                                     | Architecture exploration and literature review                                   | Completed    |                      |
| 2                                     | Testing and evaluation of previous baseline architecture                          | Completed    | [AR1][AR2]           |
| 3                                     | Modeling, characterization and design space exploration of converter topologies    | April'16     |                      |
| 4                                     | Chip tapeout-Phase I-components                                                   | May'16       |                      |
| 5                                     | Chip Testing-Phase I                                                              | Oct'16       | [AR8]                |
| 6                                     | Chip tapeout-Phase II-integrated system                                           | Nov'16       |                      |
| 7                                     | Chip Testing-Phase II                                                             | Mar'17       | [AR9][AR10]          |

| **Power supply variation in ULP systems** |                                                                                 |              |                      |
| 1                                     | Architecture exploration and literature review                                   | Completed    |                      |
| 2                                     | Exploring circuit robustness between latch vs. register based digital circuits     | Completed    | [AR4]                |
| 3                                     | All digital low-frequency droop measurement scheme                                 | Completed    | [AR4]                |
| 4                                     | Active decoupling circuit design                                                  | Nov'16       |                      |
| 5                                     | Methodology for dynamic IR drop analysis and decap insertion                       | Dec'16       | [AR12]               |

| **Characterization and demonstration of ultra low-power circuit components** |                                                                                 |              |                      |
| 1                                     | Architecture exploration and literature review                                   | Completed    |                      |
| 2                                     | ULP Microprocessor implementation in 90nm FDSOI                                    | Completed    | [AR3]                |
| 3                                     | FIR filter implementation in 55nm DDC                                              | Completed    | [AR5]                |
| 4                                     | Design space exploration of various comparator topologies for ULP wakeup receiver  | Completed    |                      |
| 5                                     | Chip tapeout for integrated wakeup-radio with ULP comparator,clocking and digital processing | May'16       |                      |
| 6                                     | Chip Testing-Wake-up-radio                                                         | Nov'16       | [AR11]               |

| Write-up                              | Thesis writing                                                                    | April'17     |                      |
Publications


Anticipated Publications


[AR6] MPPT control scheme and cold start circuit for enabling harvesting from multiple modalities
[AR7] Energy harvesting platform with cold-start, MPPT and battery supervisory circuit
[AR8] Voltage reference and bias circuits in ultra low power management units
[AR9] Supply regulation system at ultra-light-load currents
[AR10] Complete power management unit with integrated energy harvesting, supply regulation with MPPT, cold-start and battery supervision
[AR11] Ultra-low-power wakeup-radio system with ULP comparators and digital correlators
[AR12] Active decoupling capacitor circuit design and methodology for active and passive decap distribution for mitigating power supply droop.
High Level Impact

Achieve energy-autonomy, longer operational lifetime and reduce form factors in ULP SoCs

- Energy harvesting from multiple energy sources
- Supply regulation for delivering harvested power to various components of the system
- Control power supply variation
- Lower power consumption of different circuit components
References

Questions ?