Design and Analysis of the On-chip Power Delivery Network for Energy Efficient Designs

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Many applications impose energy constraints
- High Performance energy constraint:
  - Thermal
- Low Performance energy constraint:
  - Battery lifetime

Motivation

Energy efficiency is one of the largest focuses in digital integrated circuit design
Power delivery network

- Simplified model
  - Voltage generation
  - Printed circuit board (PCB)
  - Package
  - Chip

- Resistances, inductances, capacitances

Focus on the on-chip power delivery network
Prior Art

- **Dynamic voltage and frequency scaling**
  - Conventionally off-chip power delivery network optimization

- **Power gating**
  - On-chip power delivery network optimization

- **Subthreshold operation**
  - Operate below device threshold voltage ($V_T$)
  - Quadratic energy reduction, exponential performance decrease
  - Mode change i.e., infrequent voltage scaling

$$E_{op}(V_{DD}) = C_{eff}(V_{DD}) \times V_{DD}^2 + V_{DD} \times I_L(V_{DD}) \times t_{op}$$
Design challenges power delivery network

- Voltage scaling
  - Slow off-chip DC-DC converters
- $V_{DD}$ granularity
  - Shared common $V_{DD}$ across multiple cores
- IR drop
  - Voltage drop across power gates
- $di/dt$ noise
  - Rush current

**Limit the opportunity for $V_{DD}$ scaling, reducing energy efficiency**
Research goals

1. Improve voltage scaling architectures/power delivery network
   - Move $V_{DD}$ scaling from off-chip to on-chip
     - Use power switches
   - Improve $V_{DD}$ granularity

2. Enable subthreshold operation

3. Power delivery network noise analysis
   - Evaluate proposed optimizations impact
   - Propose noise mitigation techniques

4. Scripted design space exploration tool
Outline

I. Motivation
II. Background
III. Research goals

IV. Voltage scaling architectures
   I. Motivation
   II. Panoptic dynamic voltage scaling (PDVS)
   III. A programmable resistive power grid

V. Enabling subthreshold operation
VI. Power delivery network noise analysis
VII. Scripted design space exploration tool
VIII. Schedule
IX. Publications
Voltage scaling focus

- Motivation: Enable energy efficient operation
  - Move $V_{DD}$ scaling on-chip
  - Improve $V_{DD}$ granularity

- Implement PDVS [1] in a processor
  - Compare to other power delivery network optimizations

- A programmable resistive power grid
  - Leverage IR drop for energy savings
  - Create model for design
Panoptic dynamic voltage scaling

- Modify on-chip power delivery network
  - Discrete set of voltage rails
  - PMOS power switches for voltage scaling
- Fine $V_{DD}$ granularity
  - Component level
Approach

- 32 bit data flow processor
  - Adder/Multipliers attached to PMOS headers
- Fair comparison to single-$V_{DD}$, multi-$V_{DD}$

Energy savings up to 50% and 46% over single-$V_{DD}$ & multi-$V_{DD}$

Source: [2]
Programmable resistive power grid

- Monolithic header (/footer) broken into partitions \( w^k_n \)
  - Independent gate control \( \rightarrow \) control resistance
  - \( W^k \) total width
- Fewer headers on \( \rightarrow \) increased IR drop

\[
E_{op}(V_{DD}, VV_{DD}) = C_{eff}(VV_{DD}) \cdot V_{DD} \cdot VV_{DD} + V_{DD} \cdot I_L(VV_{DD}) \cdot t_{op}
\]
Multi-core model

- AMD Bulldozer core
- Route Level Macro (RLM)’s
  - Building blocks of core
  - Time dependent current source and capacitance
- Apache Redhawk
  - Commercial power integrity tool
- Simplified RLC model

Source: [3]
Model results

- Double-precision General Matric Multiply (DGEMM) benchmark
  - 25ns timing window
  - All RLMs superimposed

![Graph showing V_DD response]

V_{DD} response shows our model is properly working.

Source: [3]
Proposed contributions

- First processor implementing PDVS
  - Energy savings up to 50% and 46% over single-$V_{DD}$ & multi-$V_{DD}$
- Programmable resistive power grid
  - Leverage IR drop for energy efficiency
- Programmable resistive power grid model
  - Design, implementation and verification
Outline

I. Motivation
II. Background
III. Research goals
IV. Voltage scalable architectures
V. Enabling subthreshold operation
   I. Motivation
   II. Architecture changes in PDVS
   III. On-chip power delivery network optimizations
   VI. Power delivery network noise analysis
   VII. Scripted design space exploration tool
   VIII. Schedule
   IX. Publications
Enabling subthreshold focus

- Motivation: Enable energy efficient operation through subthreshold
  - Infrequent mode change

- Architecture modifications
  - In PDVS

- Power delivery network modifications
  - NMOS vs. PMOS for subthreshold header
  - Transmission gate vs. NMOS or PMOS for flexible designs
PDVS: Enabling subthreshold

- Added PMOS to power delivery network of:
  - Register bank
  - Crossbar

- Added bypass for component level converters
  - Level converters not designed for subthreshold operation

- Optimized level converter for subthreshold [4]
  - Converts from 0.25 up to 1.0V
  - Added bypass from data path to memories

Source: [2]
PMOS vs. NMOS

- **PMOS transistor**
  - During subthreshold operation
    \[ |V_{GS}| = V_{SUBVT} \]

- **NMOS transistor**
  - **Gate at** \( V_{DDH} \)
  - During subthreshold operation
    \[ |V_{GS}| = V_{DDH} - V_{SUBVT} \]

**NMOS provides more current**
Approach

- Commercial 130nm bulk CMOS process
- PMOS and NMOS design consisted of:
  - Varied PMOS/NMOS width
  - Ten 27-stage ring oscillators (RO) in parallel
    - Each RO can be enabled independently
    - 10 enabled => activity of 1, 1 enabled => activity of 0.1
  - $V_{DDH} => 1.2V$, $V_{SUBVT} => 0.3V$

NMOS 280X smaller than PMOS for a 10% performance degradation

Source: [4]
Transmission gate for flexibility

- Provide flexibility for designs that have a scalable $V_{DDL}$ voltage rail
  - When $V_{SUBVT} > V_T$, PMOS dominate device
  - When $V_{SUBVT} < V_T$, NMOS dominate device
- Same setup previously described
  - NMOS & PMOS width constant
  - Varied $V_{SUBVT}$ voltage

Source: [5]
Proposed contributions

- Methodology for adapting architectures for sub-threshold operation
  - PDVS used as example
- Proposed use of NMOS as subthreshold header
  - Gate at $V_{DDH}$
- Proposed use of transmission gate for flexible designs.
  - $V_{SUBVT}$ can be super or subthreshold
- Comparison between PMOS, NMOS, and transmission gate headers across $V_{DD}$
I. Motivation
II. Background
III. Research goals
IV. Voltage scalable architectures
V. Enabling subthreshold operation

VI. Power delivery network noise analysis

I. Motivation
II. Panoptic dynamic voltage scaling
III. Field programmable core array (FPCA)

VII. Scripted design space exploration tool
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Motivation: Analyze and evaluate impact of our proposed techniques on the entire power delivery network.

Synthesis and place & route approach

Analysis of physical impacts of PDVS
- $V_{\text{DD}}$ switching, i.e., $V_{\text{DDL}}$ to $V_{\text{DDH}}$
- Power grid design for varied $V_{\text{DDs}}$

Analysis of physical impacts of field programmable core array (FPCA)
- Impacts of reconfigurable architecture

Use Encounter Power System (EPS)
- Commercial power integrity tool
Synthesis and place & route approach

- **Synthesis:** behavioral RTL $\rightarrow$ structural RTL
  - Cadence RTL compiler (RC)
- **Place and route:** structural RTL $\rightarrow$ physical layout
  - Cadence Encounter

**Limitations:**
- Native support for power gating, $V_{DD}$ domains, clock gating
PDVS design approach

- Modified tool flow
  - ‘careful manipulation’
  - Scripted

- Example: PIC processor
  - ALU $\rightarrow$ 3 PMOS headers – $V_{DDH}$, $V_{DDM}$, $V_{DDL}$
  - Everything else $\rightarrow$ $V_{DDH}$
FPCA overview

- Reconfigurable architecture
- OpenRISC
  - Split into front end (FE) & processing element (PE)
  - Reconfigurable interconnect
- Variable width SIMD
- Switch between SIMD and MIMD
FPCA approach

- Synthesis and place and route flow
- Design size prohibitive
- Need tiled, scalable, hierarchical approach
  - Use interface logic module (ILM)
  - Allows us to maintain timing, speed up place & route
Encounter Power System approach

- Power delivery network integrity analysis tool
- Static and dynamic analysis
  - IR drop across power gates in PDVS & FPCA
- Rush current analysis (di/dt)
  - PDVS – switching from $V_{DDL}$ to $V_{DDH}$
  - FPCA – varying SIMD width
- Simplified RLC package model
- Design knobs
  - $V_{DD}$ voltage, metal allocation, power switch size & distribution
- Example: power gated PIC processor
  - IR map, IR histogram

Min $V_{DD}$: 1.156 V
Grid Capacitance: 0.852 pF
Proposed contributions

- PDVS synthesis and place & route flow
- Analysis and methodology for characterizing power delivery network properties associated with implementing PDVS
- Power grid design methodology for varied voltages
- Methodology for characterizing the power delivery network for reconfigurable architectures
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Tool flow focus

- **Motivation:** Need a tool flow that allows for rapid design space exploration

Current design flow

- GUI based
- Energy efficient techniques natively supported
  - Power gating, clock gating, $V_{DD}$ domains

Proposed design flow

- Scripted
- Easy to use
GUI based place and route

- Creating power grid
- Need to set many fields

For every metal layer
GUI based place and route

- Steps of place & route
  - Tool set up
    - Import: RTL, constraints, library files, LEF, etc..
  - Floor planning
  - Power planning
  - Standard cell placement
  - Clock tree synthesis
  - Routing
  - Verification

**Cumbersome, error prone, time consuming**
Proposed design tool

- Scripted
  - TCL language, perl
  - Easy to use, command line based
    - ‘launchrc.pl –powergate 0 –clockgate 1’

- Support for proposed energy efficient techniques
  - PDVS
  - Programmable resistive power grid
  - NMOS header
  - FPCA
Proposed contributions

- Scripted design tool enabling energy efficient design space exploration
- Include standard energy efficient techniques
  - Power gating
  - Clock gating
  - $V_{DD}$ domains
- Include proposed energy efficient techniques
  - PDVS
  - Programmable resistive power grid
  - NMOS header
  - FPCA
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Publications


Anticipated publications

[KAC7] PDVS JSSC journal paper
[KAC8] BSN revision2 paper.
[KAC9] PDVS noise analysis
[KAC10] Subthreshold power grid design methodologies
[KAC11] Variable width SIMD paper
[KAC12] Reconfigurable architecture noise analysis
[KAC13] Energy efficient tool paper
References


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