VLSI Project Proposal – Priority Encoder

Yukang Feng and Xiaoyu Wang

I. Visions and Goals

In todays digital circuit applications, as an enhancement of simple encoder circuit, the priority encoder (PE) works as an indispensible logic component in VLSI systems. It could pass priority taken from highest priority to the lowest priority to realize necessary functions. The application of priority encoder is observed in the design of content addressable memories, data bus, comparators, incrementer/decrementers and so on. The significance of more advanced PE design is simple: to realize indispensible logic function in simpler structure while keep a lower energy consumption and higher speed functioning

A. Overview of PEs and Their Applications

A PE is significantly different from the one commonly called Binary Encoder (BE), which takes all its data inputs one at a time and then converts them into a single encoded output. In comparison, PE only encoding the highest order lines. PE is widely applied as necessary part in various components. Not only to realize the function, but also help to realize lower power consumption and shorter system delay.

Previously, an energy-efficient adaptive hybrid cache was introduced [1]. With PE as part of its functional part, it could realize an adaptive mapping scheme to reduce time consumption in searching physical address by 20% to 40%. In a leakage energy reduction addressable memory design [2], a bank structure compressed of buffers, priority encoders and address decoders reduced the complexity of the memorys logic structure. This saves area, power consumption and improves the delay of these devices. As a result, the leakage power consumption is also minimized by 90% with active area is decreased by 10%. In a low power Ternary content addressable memories (TCAM) design, PE was used to build up double Pai-Sigma match lines, which helped to reduce power consumption by 60%.

B. Purposes of the Project

As a widely used component of VLSI system, we always want to design a simpler PE with shorter propagation time and lower energy cost for optimized VLSI in characteristics of delay, energy consumption and complexity.

- In this project, we would first review existed PE designs in metrics of propagation delay, energy consumption and circuit structure complicity.
- On basis of cadence simulation under 45 nm technology, we would compare their performance and find out the optimized PE circuit structure.
- Then, we would make efforts to make further improvement.

II. State-of-the-Art PE designs

Previously, variety of research was conducted to improve the performance of PE. In existed research, different topology and sizing were introduced on basis of available fabrication technologies.

A multilevel look-ahead structure is developed to shorten the critical path [4]. Such look-ahead structure is realized by NP Domino logic and parallel-connected circuit structure. For a high-speed application while maintain low power consumption, a series-connected circuit structure introduced to reduce switching activity. Later, on basis of simple look-ahead structure, a Multilevel folding technique was reported in [5], which could reduce the delay to the order of $\mathcal{O}\left(\log_2 \mathrm{N}\right)$. In this paper, both the multilevel look-ahead and the multilevel folding techniques were proved to be easily merged and implemented in the dynamic CMOS circuits. Multilevel Folding method could significantly reduce the power dissipation and propagation delay.

However, its structure is considerably complex and the look-ahead signal routing is highly irregular. To solve such problem, power-optimized 8-bit priority encoder cell [6] is presented. This structure simplifies the transistor number from 102 to 62. Meanwhile, the delay was also reduced by a parallel priority look-ahead architecture. An enhanced priority encoder FPPE was introduced in the comparator circuitry [7]. FPPE brought a better performance in energy consumption, which was also inherited by a Power, delay and area optimized 8-bit CMOS priority encoder [8] to realize a design with less transistor number.

III. Problem Identification and Approaches

A. Unsolved Issues and Thoughts

Previous research provided different approaches to realize better PE performance. However, after a carefully inspection, we find certain ambiguities in such designs which need to be further clarified. The first question is: how would those existed designs function under cutting edge technology? For example, design [4], [5] and [6] were realized on basis of 600 nm technology; design [8] and [9] used 250 nm technology; in design [7], implementation was realized by 90 nm technology. The structure designs of PE in above are inspiring and their reliability was proved by previous applications. Could we apply their topology in a more advanced 45nm technology? As we know, the 45 nm technology was mass-producing since 2010, and it is still the workhorse in industry for chip fabrication now. In our project, we would rebuild the relative circuits in cadence using 45 nm technology to test their function.

To optimize PEs performance in design, we want to find out the best design existed and make further improvement from there. How to find out the best? It seems the newest design is always more advanced and it was even convinced by data comparing with older designs. However, is this improvement a result of better circuit structure design or it is simply profited from newest semiconductor technology (for example, [8] claimed a better performance than [5], however, [8] utilized 250 nm technology while [5] was implemented under 600 nm technology). Whats more, reported improvements of some designs are not comprehensive. For example, certain design just provided the improvement in energy consumption, however, it did not provide its performance in delay. Which make the claimed improvement suspicious.

In our project, an equal competition would be presented to find out the best circuit structure design considering energy consumption, propagation delay and simplicity of topology. On basis of that, we would make efforts to further optimize the circuit structure and try to provide a more advanced design.

B. Identified Questions and Potential Approaches

Q1: Which existed PE(s) has the optimal performance in terms of delay, power consumption or/and area? (Research component & Simulations)

First we will implement a series of PEs proposed in previous papers within the same framework, i.e., using the same NCSU_Devices_FreePDK45 library to verify their feasibility with the new technology (related simulation results are provided in Section IV). Furthermore, their delay and power consumption could be measured directly and conveniently using built-in tools (Calculator and Results Browser) in Cadence, based on which their performance in terms of delay, power consumption and complexity could be compared fairly and precisely.

Q2: Could the three metrics be further improved by designing new PE structure? (Design component & Simulations)

We will try to modify the architecture of existed PEs aiming to reducing delay, power dissipation or/and circuit area.

Q3: How accurate could we predict a PEs delay and power-consumption performance by deriving formulas? (Research component & Simulations)

We plan to extract parasitic capacitances and resistances of PEs using Cadence and then derive formulas for best- and worst-case propagation delays and power consumption. Afterwards, we will compare the results from formulas and simulations to answer the question.

If we have extra time, the following questions will also be explored:

Q4: Whether a delay-optimizaed 8-bit PE could achieve optimal delay performance when applied to the design of a 32-bit or 64-bit PE? If not, how could we design a 64-bit PE with smaller delay? (Research component & Simulations)

We plan to use the 8-bit PEs in Q1 to comprise higher-bit PEs and then compare their delay or/and power performance via simulations. The numerical results will help us to find out the answer whether a 8-bit PE with shortest delay will contribute to a optimal 32- or 64-bit PE.

Q5: Could we design a 64-bit PE with smaller power consumption using 8-bit PEs? (Design component & Simulations) By taking into account the differences between a 8-bit PE and a higher-bit PE, we would try to design a new structure for a 32- or 64-bit PE to achieve better delay performance.

IV. Simulation Results & Novelties

A. Simulation Results

Simulation results (timing diagrams) of three previously proposed PEs (Full Parallel PE, Power-Delay-Area-Optimized PE and Active-Low PE) are provided at the end of the proposal.

B. Novelties

- **Fairly compare the previous design:** This would be a new idea to put different PE designs under the same fabrication technology in simulation. In this way, the performance competition of circuit structure designs will be equal. This is important because we can find out the optimized circuit structure, which could be used as precious reference in future design.
- **A comprehensive review will be represented in this project:** Some existed design would prefer to compare other designs on their advantaged features, and keep their potential weakness ambiguous. In this project, we would compare all three significant characteristics of PE: propagation delay, energy consumption and circuit complicity. The result would be given clearly in chart.
- **Cutting edge technology will be applied in our new design:** To make the PE design useful for application, we utilized the cutting-edge 45 nm technology which is widely used in industry recently.
- **Mathematical approach will be given for energy consumption & propagation delay estimation:** In this project, we want to provide useful mathematical estimation approach. Such approach could helper future developers to work on improving performance of PE as well as other components.

V. Timeline and Task Breakdown

TABLE I
Timeline

Oct. 17 - Oct. 31	Q1: repeat existed PEs in the papers and compare their performance
Nov. 1 - Nov. 10	Q2: try to design a new PE with better performance
Nov. 11 - Nov. 23	Q3: formula derivation and results comparison
Nov. 24 - Dec. 2	Q4 & Q5: 32-bit or 64-bit PEs

Task Breakdown:

- Q1: YF - literature search and report writing, XW - simulation
- Q2: YF & XW - PE design and simulation
- Q3: XW - formula derivation, YF - simulation
- Q4 & Q5 - PE design and simulation
- Reports and final presentation: YF & XW.